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PATENT APPLICATION

ATTORNEY DOCKET NO. 10014282-1

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	Andrew Spencer	Confirmation No.:	3876
Application No.:	10/689,244	Examiner:	Chun Cao
Filing Date:	Oct. 20, 2003	Group Art Unit:	2115

Title: SYSTEM AND METHOD FOR SETTING A CLOCK RATE OF A MEMORY CARD

Mail Stop Appeal Brief-Patents
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF

Transmitted herewith is the Appeal Brief in this application with respect to the Notice of Appeal filed on Dec. 17, 2007.

☐ The fee for filing this Appeal Brief is $510.00 (37 CFR 41.20).

☐ No Additional Fee Required.

☒ Additional fee of $10 to cover the difference between the current Appeal Brief filing fee ($510) and the previously paid Appeal Brief filing fee ($500).

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

☐ 1st Month $120	☐ 2nd Month $460	☐ 3rd Month $1050	☐ 4th Month $1640

☐ The extension fee has already been filed in this application.

☒ (b) Applicant believes that no extension of time is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account 08-2025 the sum of $ 10.00. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees.

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Respectfully submitted,

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant:	Andrew Spencer	Examiner: Chun Cao
Serial No.:	10/689,244	Group Art Unit: 2115
Filed:	Oct. 20, 2003	Docket No.: 10014282-1
Due Date:	Feb. 17, 2008	
Title:	SYSTEM AND METHOD FOR SETTING A CLOCK RATE OF A MEMORY CARD	

APPEAL BRIEF UNDER 37 C.F.R. §41.37

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This Appeal Brief is submitted in support of the Notice of Appeal filed on December 17, 2007, appealing the final rejection of claims 1, 2, 4-20, and 24-36 of the above-identified application as set forth in the Final Office Action mailed October 24, 2007.

The U.S. Patent and Trademark Office is hereby authorized to charge Deposit Account No. 08-2025 in the amount of $10.00 to cover the difference between the current fee for filing a Brief in Support of an Appeal as set forth under 37 C.F.R. §41.20(b)(2) ($510) and the previously paid fee for filing a Brief in Support of an Appeal ($500). At any time during the pendency of this application, please charge any required fees or credit any overpayment to Deposit Account No. 08-2025.

Appellant respectfully requests consideration and reversal of the Examiner's rejection of pending claims 1, 2, 4-20, and 24-36.

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REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, LP having a principal place of business at 20555 S.H. 249 Houston, TX 77070, U.S.A. (hereinafter "HPDC"). HPDC is a Texas limited partnership and is a wholly-owned affiliate of Hewlett-Packard Company, a Delaware corporation, headquartered in Palo Alto, CA. The general or managing partner of HPDC is HPQ Holdings, LLC.

RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellant that will have a bearing on the Board's decision in the present Appeal.

STATUS OF CLAIMS

In a Final Office Action mailed Oct. 24, 2007, claims 1, 2, 4-20, and 24-36 were finally rejected. Claims 1, 2, 4-20, and 24-36 are pending in the application and are the subject of the present Appeal.

STATUS OF AMENDMENTS

No amendments have been entered subsequent to the Final Office Action mailed October 24, 2007.

SUMMARY OF THE CLAIMED SUBJECT MATTER

Discussions about elements of independent claims 1, 10, 19, 28, and 33 can be found at least at the cited locations in the specification and drawings.

Independent claim 1 claims a memory card. The memory card includes a buffer configured to receive transactions, a storage media, a control circuit coupled to the buffer and the storage media, a processor system coupled to the control circuit, and a buffer management circuit coupled to the processor system and configured to provide at least one signal to the processor system that indicates when the buffer is full and when the buffer is empty. The processor system is configured to detect a rate of transactions received by the buffer by determining a number of times that the buffer is full and empty from the at least one signal over a time period. The control circuit is configured to cause a first clock signal to be provided to the buffer and the storage media at a first clock rate that varies in dependence on the detected rate of the transactions. See, e.g., p. 3, lines 6-9, 20-22 and 26-27; p. 5, lines 28-31; p. 6, lines 3-13; p. 7, lines 10-23; Figure 1, reference numbers 120, 134, 136, 138, and 150; Figure 2, reference numbers 204 and 206; Figure 3, reference number 120.

Independent claim 10 claims a system. The system includes a host device and a memory card configured to couple to the host device. The memory card includes a storage media. The memory card is configured to count a number of transactions received by the memory card from the host device during a time period and to provide a first clock signal to the storage media at a first clock rate that varies in dependence on the number of transactions received by the memory card from the host device during the time period. See, e.g., p. 2, lines 25-31; p. 3, lines 6-9, 20-22 and 26-27; p. 6, lines 3-6; p. 7, lines 1-8 and 10-23; Figure 1, reference numbers 110, 120, 134, 136, 138, and 150; Figure 2, reference numbers 204 and 206; Figure 3, reference number 120 and 310.

Independent claim 19 claims a method. The method includes determining a first rate of transactions received by a buffer in a memory card by comparing an amount of information stored in the buffer to a threshold level, setting a first clock signal of the memory card to a first clock rate that varies in dependence on the rate of transactions, and providing the first clock signal the buffer and a storage media in the memory card. See, e.g., p. 3, lines 6-9, 20-22 and 26-27; p. 6, lines 3-6 and 14-31; p. 7, lines 10-23; Figure 1, reference numbers

120, 134, 136, 138, and 150; Figure 2, reference numbers 204 and 206; Figure 3, reference number 120.

Independent claim 28 claims a memory card. The memory card includes a buffer configured to receive transactions, a storage media, a clock configured to generate a clock signal and provide the clock signal to the buffer and the storage media, a means for counting a number of the transactions received by the buffer over a time period (Figure 1, reference numeral 134), and a means for causing the clock signal to be set at a rate associated with the number of transactions (Figure 1, reference numerals 134 and /or 138). See, e.g., p. 3, lines 6-9, 20-22 and 26-27; p. 4, lines 20-23; p. 6, lines 3-6; p. 7, lines 1-8 and 10-23; Figure 1, reference numbers 120, 134, 136, 138, and 150; Figure 2, reference numbers 204 and 206; Figure 3, reference number 120.

Independent claim 33 claims a memory card. The memory card includes a buffer, an interface configured to receive transactions from a host device and provide the transactions to the buffer, a storage media, a control circuit coupled to the buffer and the storage media, and a processor system coupled to the control circuit. The processor system is configured to count a number of transactions received by the buffer over a time period. The processor system is configured to cause the control circuit to set a first clock signal to a first clock rate that varies in dependence on the number of transactions received by the buffer. The control circuit is configured to cause the first clock signal to be provided to the buffer and the storage media. See, e.g., p. 3, lines 6-9, 18-22 and 26-27; p. 4, lines 20-23; p. 6, lines 3-6; p. 7, lines 1-8 and 10-23; Figure 1, reference numbers 120, 132, 134, 136, 138, and 150; Figure 2, reference numbers 204 and 206; Figure 3, reference number 120.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Claims 1, 2, and 4-9 stand rejected under 35 U.S.C. §112, first paragraph as failing to comply with the enablement requirement.

II. Claims 10-20 and 24-36 stand rejected under 35 U.S.C. § 103(a).

ARGUMENT

I. Rejection of Claims 1, 2, and 4-9 under 35 U.S.C. § 112, first paragraph

A. The Applicable Law

35 U.S.C. § 112, first paragraph, states:

> The specification shall contain a written description of the invention, and the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

B. Rejection of Claim 1 under 35 U.S.C. § 112, first paragraph

The Examiner rejected claim 1 under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The Examiner alleged that "the newly added limitation 'by determining a number of times that (sic) buffer is full and empty from the at least one signal over a time period' is not described in the specification." Office Action of October 24, 2007, p. 2, paragraph 5.

Claim 1 recites, *inter alia*:

> wherein the processor system is configured to detect a rate of transactions received by the buffer by determining a number of times that the buffer is full and empty from the at least one signal over a time period … .

Applicants respectfully submit that the above limitations of claim 1 are fully described in at least the following portions of the Specification. In paragraph [0013], p. 3, lines 26-27, the Specification teaches the following.

> Buffer and buffer management circuit 136 provides buffer empty / buffer full signals to processor system 134 using one or more lines 158.

In addition, the Specification, in paragraph [0022], p. 6, lines 6-13, teaches that:

> processor system 134 may determine the rate of transactions by monitoring how quickly the buffer in buffer and buffer management 136 fills and empties. To do so, processor system 134 monitors the number of times that it receives a buffer full signal and / or buffer empty signal from buffer and buffer management 136 over one or more time periods. Buffer and buffer

> management 136 generates the buffer full signal to indicate that the buffer is full and generates the buffer empty signal to indicate that the buffer is empty.

Because these portions of the Specification fully describe the above limitations of claim 1, Applicants respectfully submit that claim 1 fully complies with 35 U.S.C. § 112, first paragraph. Accordingly, Applicants respectfully request reversal of the rejection of claim 1 under 35 U.S.C. § 112, first paragraph.

C. Rejection of Claims 2 and 4-9 under 35 U.S.C. § 112, first paragraph

The Examiner rejected claims 2 and 4-9 under 35 U.S.C. § 112, first paragraph, based on the rejection of claim 1. Because claim 1 fully complies with 35 U.S.C. § 112, first paragraph, as described above, Applicants respectfully request reversal of the rejection of claims 2 and 4-9 under 35 U.S.C. § 112, first paragraph.

II. Rejection of Claims 10-20 and 24-36 under 35 U.S.C. § 103(a)

A. The Applicable Law

The Examiner has the burden under 35 U.S.C. §103 to establish a *prima facie* case of obviousness. *In re Fine,* 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Three criteria must be satisfied to establish a *prima facie* case of obviousness. First, the Examiner must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would teach, suggest, or motivate one to modify a reference or to combine the teachings of multiple references. *Id.* Second, the prior art can be modified or combined only so long as there is a reasonable expectation of success. *In re Merck & Co., Inc.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Third, the prior art reference or combined prior art references must teach or suggest all of the claim limitations. *In re Royka,* 490 F.2d 981, 180 USPQ 580 (CCPA 1974). These three criteria are also set forth in §706.02(j) of the M.P.E.P. In performing the obviousness inquiry under 35 U.S.C. §103, the Examiner must avoid hindsight. *In re Bond,* 910 F.2d 831, 834, 15 USPQ2d 1566, 1568 (Fed. Cir. 1990), *reh'g denied*, 1990 U.S. App. LEXIS 19971 (Fed. Cir. 1990).

B. Rejection of Claims 10-18 and 28-36 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,407,940[1] to Aizawa et al. ("Aizawa") in view of U.S. Patent No. 4,288,860 to Trost ("Trost")

Neither Aizawa nor Trost, alone or in combination, teach or suggest all of the claim limitations of claims 10-18 and 28-36.

1. Claims 10-18

Claim 10 recites *inter alia*:

> a host device; and
> a memory card configured to couple to the host device;
> wherein the memory card includes a storage media, wherein the memory card is configured to count a number of transactions received by the memory card from the host device during a time period, and wherein the memory card is configured to provide a first

[1] Applicants respectfully note that Aizawa refers to U.S. Patent No. 6,407,940 and not U.S. Patent No. 6,407,941 as indicated in the Final Office Action mailed October 24, 2007. *See* Notice of References Cited (PTO-892) from the Office Action mailed April 17, 2006.

> clock signal to the storage media at a first clock rate that varies in dependence on the number of transactions received by the memory card from the host device during the time period.

Neither Aizawa nor Trost teach or suggest "wherein the memory card is configured to count a number of transactions received by the memory card from the host device during a time period, and wherein the memory card is configured to provide a first clock signal to the storage media at a first clock rate that varies in dependence on the number of transactions received by the memory card from the host device during the time period" as recited in claim 10.

The Examiner concedes that Aizawa does not teach or suggest does not teach or suggest these limitations of claim 10. Final Office Action mailed October 24, 2007, p. 3 (hereafter "Final Office Action").

Trost also does not teach or suggest these limitations of claim 10. In particular, Trost does not teach or suggest "count[ing] a number of transactions received …during a time period " or "provid[ing] a first clock signal … at a first clock rate that varies in dependence on the number of transactions received … during the time period" as recited in claim 10.

Trost teaches transferring data between a dynamic storage subsystem (storage 10) and a requestor 11 using register stack 21 that functions as a FIFO buffer. Trost, col. 1, line 50 to col. 2, line 14, col. 3, lines 1-16 and Figures 1 and 2. Trost teaches that "[d]uring the time that data is being transferred to and from the FIFO buffer, the frequency of the variable rate oscillator is determined by *the amount of data currently resident in the FIFO buffer*." Trost, col. 2, lines 14-17 (emphasis added).

Trost teaches that clock control 24 determines the oscillator rate of the variable rate oscillator. Trost, col. 3, lines 56-57. With reference to clock control 24 in Figure 4, Trost teaches that:

> [T]he oscillator rate is determined by OR-gates 324, 333, 337, and 329. … [I]f the output of all four OR-gates … are high, … the variable rate oscillator operates at the maximum (2.5 megahertz) rate. Similarly, the output of all four OR-gates are low, … the variable rate oscillator operates at the minimum (1.0 megahertz) rate. Col. 5, line 60 to col. 6, line 7.

Trost further teaches that:

> [i]t can be seen that the four control flip-flops [i.e., FF4 308, FF5 309, FF6 310, and FF7 311], therefore, maintain a record of which of the four 32-bit registers of REGISTER STACK 21 currently contain data which is being buffered for output. Stated another way, the four control flip-flops maintain a record of which of the four 32-bit registers of REGISTER STACK 21 are in use. For write accesses, the frequency of the variable rate oscillator will be increased as the number of 32-bit registers in use is increased and will be decreased as the number of 32-bit registers in use is decreased. Conversely, for read accesses, the frequency of the variable rate oscillator will be decreased as the number of 32-bit registers in use is increased and will be increased as the number of 32-bit registers in use is decreased. Col. 6, line 60 to col. 7, line 6.

Accordingly, Trost teaches that the oscillator rate varies in response to which registers of register stack 21 are in use.

Claim 10 recites "wherein the memory card is configured to count a number of transactions received by the memory card from the host device during a time period … ." Trost does not teach or suggest that clock control 24 "count[s] a number of transactions received … during a time period" as recited in claim 10. Instead, Trost monitors which registers in register stack 21 are in use at any given instant and does not track which registers are used over a time period.

The Examiner cites col. 4, lines 18-37 and 58-65 and Figure 2 of Trost as a teaching or suggestion of this limitation of claim 10. Final Office Action, p. 3. These teachings of Trost describe the construction of register stack 21 – a FIFO buffer (col. 4, lines 18-37 and Figure 2) and register control 23 – circuitry that operates a FIFO buffer (col. 4, lines 58-65). These portions of Trost do not teach or suggest the above limitation of claim 10.

Claim 10 also recites "wherein the memory card is configured to provide a first clock signal to the storage media at a first clock rate that varies in dependence on the number of transactions received by the memory card from the host device during the time period … ." As described above, Trost does not count a number of transactions received during a time period. Accordingly, Trost also does not teach or suggest that clock control 24 "provide[s] a first clock signal … at a first clock rate that varies in dependence on the number of transactions received … during the time period" as recited in claim 10.

The Examiner cites Figure 1, the abstract, and col. 2, lines 3-34, col. 3, line 56 to col. 4, line 16, and col. 7, line 65 to col. 8, line 10 of Trost as a teaching or suggestion of this limitation of claim 10. Final Office Action, p. 3. None of these portions of Trost teach or suggest the above limitation of claim 10.

Because neither Aikawa nor Trost teach or suggest all limitations of claim 10, the Examiner has not set forth a *prima facie* case of obviousness under 35 U.S.C. § 103(a). Accordingly, Applicants respectfully request the reversal of the rejection of claim 10, and claims 11-18 which depend from claim 10, under 35 U.S.C. §103(a) for at least the above reasons.

2. Claim 28-32

Claim 28 recites *inter alia*:

> a buffer configured to receive transactions;
> a storage media;
> a clock configured to generate a clock signal and provide the clock signal to the buffer and the storage media;
> means for counting a number of the transactions received by the buffer over a time period; and
> means for causing the clock signal to be set at a rate associated with the number of transactions.

Neither Aizawa nor Trost teach or suggest "means for counting a number of the transactions received by the buffer over a time period" or "means for causing the clock signal to be set at a rate associated with the number of transactions" as recited in claim 28.

To reject claim 28, the Examiner refers to the rejection of claims 10-18. Final Office Action, p. 5. The Examiner appears to concede that Aikawa does not teach these limitations of claim 23. *See* Final Office Action, p. 3.

As described above with reference to claim 10, Trost does not teach or suggest that clock control 24 "count[s] a number of transactions received … over a time period" as recited in claim 10. Instead, clock control 24 of Trost monitors which registers in register stack 21 are in use at any given instant and does not track which registers are used over a time period. Accordingly, Trost also does not teach or suggest "means for causing the clock signal to be set at a rate associated with the number of transactions" as recited in claim 28. The portions

of Trost cited by the Examiner do not provide any teaching or suggestion of the above features of claim 28.

Because neither Aikawa nor Trost teach or suggest all limitations of claim 28, the Examiner has not set forth a *prima facie* case of obviousness under 35 U.S.C. § 103(a). Accordingly, Applicants respectfully request the reversal of the rejection of claim 28, and claims 29-32 which depend from claim 28, under 35 U.S.C. §103(a) for at least the above reasons.

3. Claim 33-36

Claim 33 recites *inter alia*:

> a buffer;
> an interface configured to receive transactions from a host device and provide the transactions to the buffer;
> a storage media;
> a control circuit coupled to the buffer and the storage media; and
> a processor system coupled to the control circuit;
> wherein the processor system is configured to count a number of transactions received by the buffer over a time period, wherein the processor system is configured to cause the control circuit to set a first clock signal to a first clock rate that varies in dependence on the number of transactions received by the buffer, and wherein the control circuit is configured to cause the first clock signal to be provided to the buffer and the storage media.

Neither Aizawa nor Trost teach or suggest "wherein the processor system is configured to count a number of transactions received by the buffer over a time period" or "wherein the processor system is configured to cause the control circuit to set a first clock signal to a first clock rate that varies in dependence on the number of transactions received by the buffer" as recited in claim 33.

To reject claim 33, the Examiner refers to the rejection of claims 10-18. Final Office Action, p. 5. The Examiner appears to concede that Aikawa does not teach these limitations of claim 23. *See* Final Office Action, p. 3.

As described above with reference to claim 10, Trost does not teach or suggest that clock control 24 "count[s] a number of transactions received … over a time period" as recited

in claim 33. Instead, Trost monitors which registers in register stack 21 are in use at any given instant and does not track which registers are used over a time period. Accordingly, Trost also does not teach or suggest "wherein the processor system is configured to cause the control circuit to set a first clock signal to a first clock rate that varies in dependence on the number of transactions received by the buffer" as recited in claim 33. The portions of Trost cited by the Examiner do not provide any teaching or suggestion of the above features of claim 33.

Because neither Aikawa nor Trost teach or suggest all limitations of claim 33, the Examiner has not set forth a *prima facie* case of obviousness under 35 U.S.C. § 103(a). Accordingly, Applicants respectfully request the reversal of the rejection of claim 33, and claims 34-36 which depend from claim 33, under 35 U.S.C. §103(a) for at least the above reasons.

C. Rejection of Claims 19, 20, and 24-27 under 35 U.S.C. § 103(a) as being unpatentable over Aizawa in view of Trost in further view of U.S. Patent No. 6,990,598 to Sherburne ("Sherburne")

Aizawa, Trost, and Sherburne, alone or in combination, do not teach or suggest teach or suggest all of the claim limitations of claims 19, 20, and 24-27.

Claim 19 recites *inter alia*:

> determining a first rate of transactions received by a buffer in a memory card by comparing an amount of information stored in the buffer to a threshold level;
>
> setting a first clock signal of the memory card to a first clock rate that varies in dependence on the rate of transactions; and
>
> providing the first clock signal to the buffer and a storage media in the memory card.

None of Aizawa, Trost, and Sherburne teach or suggest "determining a first rate of transactions received by a buffer in a memory card by comparing an amount of information stored in the buffer to a threshold level" or "setting a first clock signal of the memory card to a first clock rate that varies in dependence on the rate of transactions" as recited in claim 19.

The Examiner concedes that Aizawa and Trost do not teach or suggest does not teach or suggest "determining a first rate of transactions received by a buffer in a memory card by

comparing an amount of information stored in the buffer to a threshold level" as recited in claim 19. Final Office Action, p. 6.

In addition, neither Aizawa nor Trost teach or suggest "setting a first clock signal of the memory card to a first clock rate that varies in dependence on the rate of transactions" as recited in claim 19. As noted by the Examiner with reference to claim 1, Aizawa does not teach "generating a clock signal at a clock rate [that] (sic) varies in dependence on a number of transactions received … during a time period." Final Office Action, p. 3. Similarly, Aizawa does not teach or suggest the above limitation of claim 19.

Further to the arguments described above with reference to claims 10, 28, and 33, Trost does not teach or suggest that clock control 24 "determine[s] a first rate of transactions" as recited in claim 19. Instead, Trost monitors which registers in register stack 21 are in use at any given instant and does not track which registers are used over a time period. Accordingly, Trost also does not teach or suggest "setting a first clock signal of the memory card to a first clock rate that varies *in dependence on the rate of transactions*" as recited in claim 19 (emphasis added).

Sherburne also does not teach or suggest the above limitations of claim 19.

In the portions of Sherburne cited by the Examiner Sherburne teaches that "[t]he method can vary the clock input to the processor and the second buffer based on the *fill status* of the second buffer further comprises slowing down or stopping the clock *if the second buffer is above its high water mark or if the buffer is full*." Sherburne, col. 3, lines 8-23 (emphasis added); *see also* col. 7, lines 6-13 and col. 8., lines 30-37. Thus, Sherburne teaches determining a *fill status* of the buffer and not "determining a first *rate of transactions* received by a buffer in a memory card by comparing an amount of information stored in the buffer to a threshold level" as recited in claim 19 (emphasis added). Accordingly, Sherburne does not teach or suggest this limitation of claim 19.

Because Sherburne does not teach or suggest "determining a first rate of transactions", Sherburne also does not teach or suggest "setting a first clock signal of the memory card to a first clock rate that varies in dependence on the *rate of transactions*" as recited in claim 19 (emphasis added). Sherburne, instead, teaches that the clock input to the processor is varied based on the fill status of the buffer

Because none of Aizawa, Trost, and Sherburne teach or suggest all limitations of claim 19, the Examiner has not set forth a *prima facie* case of obviousness under 35 U.S.C. § 103(a). Accordingly, Applicants respectfully request the reversal of the rejection of claim 19, and claims 20 and 24-27 which depend from claim 19, under 35 U.S.C. §103(a) for at least the above reasons.

CONCLUSION

For the above reasons, Appellants respectfully submit that the claims are fully supported by the Specification and that the cited references do not render the claims of the pending Application obvious. Accordingly, Appellants respectfully request that the Examiner be reversed and that claims 1, 2, 4-20, and 24-36 be allowed.

Any inquiry regarding this Response should be directed to Manisha Chakrabarti at Telephone No. (630) 355-3376 or Christopher P. Kosh at Telephone No. (512) 241-2403. In addition, all correspondence should continue to be directed to the following address:

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Dated: February 14, 2008
CPK:dmd

/Christopher P. Kosh/
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CLAIMS APPENDIX

1. (Previously Presented) A memory card comprising:

a buffer configured to receive transactions;

a storage media;

a control circuit coupled to the buffer and the storage media; and

a processor system coupled to the control circuit;

a buffer management circuit coupled to the processor system and configured to provide at least one signal to the processor system that indicates when the buffer is full and when the buffer is empty;

wherein the processor system is configured to detect a rate of transactions received by the buffer by determining a number of times that the buffer is full and empty from the at least one signal over a time period, and wherein the control circuit is configured to cause a first clock signal to be provided to the buffer and the storage media at a first clock rate that varies in dependence on the detected rate of the transactions.

2. (Previously Presented) The memory card of claim 1 wherein the processor system is configured to cause the control circuit to set the first clock signal to the first clock rate associated with the rate of transactions received by the buffer.

3. (Canceled)

4. (Original) The memory card of claim 2 further comprising:

a master clock configured to provide a second clock signal at a second clock rate to the processor system and the control circuit;

wherein the control circuit is configured to generate the first clock signal using the second clock signal.

5. (Original) The memory card of claim 4 wherein the first clock rate differs from the second clock rate.

6. (Original) The memory card of claim 1 further comprising:

a first interface coupled to the buffer and configured to receive the transactions from a host device and provide the transactions to the buffer; and

a second interface coupled to the buffer and the storage media.

7. (Original) The memory card of claim 1 wherein the transactions include read transactions configured to cause information to be read from the storage media.

8. (Original) The memory card of claim 1 wherein the transactions include write transactions configured to cause information to be written to the storage media.

9. (Original) The memory card of claim 1 wherein the transactions include read transactions configured to cause information to be read from the storage media and write transactions configured to cause information to be written to the storage media.

10. (Previously Presented) A system comprising:

a host device; and

a memory card configured to couple to the host device;

wherein the memory card includes a storage media, wherein the memory card is configured to count a number of transactions received by the memory card from the host device during a time period, and wherein the memory card is configured to provide a first clock signal to the storage media at a first clock rate that varies in dependence on the number of transactions received by the memory card from the host device during the time period.

11. (Previously Presented) The system of claim 10 wherein the memory card includes a processor system and a control circuit coupled to the processor system, wherein the processor system is configured to count the number of transactions received by the memory card from the host device during the time period, and wherein the processor system is configured to cause the control circuit to set the rate of the first clock signal in response to the number of transactions.

12. (Previously Presented) The system of claim 11 wherein the memory card includes a buffer and a buffer management circuit, wherein the buffer management circuit is configured to provide information to the processor system, and wherein the processor system is configured to count the number of transactions received by the memory card during the time period using the information.

13. (Original) The system of claim 11 wherein the memory card includes a clock configured to provide a second clock signal to the processor system and the control circuit at a second clock rate, and wherein the control circuit is configured to generate the first clock signal using the second clock signal.

14. (Original) The system of claim 10 wherein host device comprises a digital camera.

15. (Original) The system of claim 10 wherein the memory card includes a buffer and an interface coupled to the buffer, and wherein the interface is coupled to receive the transactions from the host device and provide the transactions to the buffer.

16. (Original) The system of claim 10 wherein the transactions include read transactions configured to cause information to be read from the memory card and provided to the host device.

17. (Original) The system of claim 10 wherein the transactions include write transactions configured to cause information to be written from the host device to the memory card.

18. (Original) The system of claim 10 wherein the transactions include read transactions configured to cause first information to be read from the storage media and provided to the host device and write transactions configured to cause second information to be written from the host device to the memory card.

19. (Previously Presented) A method comprising:

determining a first rate of transactions received by a buffer in a memory card by comparing an amount of information stored in the buffer to a threshold level;

setting a first clock signal of the memory card to a first clock rate that varies in dependence on the rate of transactions; and

providing the first clock signal to the buffer and a storage media in the memory card.

20. (Previously Presented) The method of claim 19 further comprising:

determining the first rate of transactions by monitoring the buffer of the memory card.

21-23. (Canceled)

24. (Original) The method of claim 19 further comprising:

subsequent to determining the first rate, determining a second rate of transactions received by the memory card; and

setting the first clock signal to a second clock rate associated with the rate of transactions.

25. (Original) The method of claim 19 wherein the transactions include read transactions configured to cause information to be read from the memory card.

26. (Original) The method of claim 19 wherein the transactions include write transactions configured to cause information to be written to the memory card.

27. (Original) The method of claim 19 wherein the transactions include read transactions configured to cause first information to be read from the memory card and write transactions configured to cause second information to be written to the memory card.

28. (Previously Presented) A memory card comprising:

a buffer configured to receive transactions;

a storage media;

a clock configured to generate a clock signal and provide the clock signal to the buffer and the storage media;

means for counting a number of the transactions received by the buffer over a time period; and

means for causing the clock signal to be set at a rate associated with the number of transactions.

29. (Original) The memory card of claim 28 further comprising:

an interface coupled to the buffer;

wherein the interface is configured to receive the transactions from a host device and provide the transactions to the buffer.

30. (Original) The memory card of claim 28 wherein the transactions include read transactions configured to cause information to be read from the storage media.

31. (Original) The memory card of claim 28 wherein the transactions include write transactions configured to cause information to be written to the storage media.

32. (Original) The memory card of claim 28 wherein the transactions include read configured to cause information to be read from the storage media and write transactions configured to cause information to be written to the storage media.

33. (Previously Presented) A memory card comprising:

a buffer;

an interface configured to receive transactions from a host device and provide the transactions to the buffer;

a storage media;

a control circuit coupled to the buffer and the storage media; and

a processor system coupled to the control circuit;

wherein the processor system is configured to count a number of transactions received by the buffer over a time period, wherein the processor system is configured to cause the

control circuit to set a first clock signal to a first clock rate that varies in dependence on the number of transactions received by the buffer, and wherein the control circuit is configured to cause the first clock signal to be provided to the buffer and the storage media.

34. (Original) The memory card of claim 33 further comprising:

a master clock configured to provide a second clock signal at a second clock rate to the processor system and the control circuit;

wherein the control circuit is configured to generate the first clock signal using the second clock signal.

35. (Original) The memory card of claim 33 wherein the transactions include read transactions configured to cause information to be read from the storage media.

36. (Original) The memory card of claim 33 wherein the transactions include write transactions configured to cause information to be written to the storage media.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.